WHAT IS CLAIMED IS:

1. An integrated circuit, comprising:

a semiconductor die including at least one pair of bond pads, each pair of bond pads having a single corresponding bond wire connected thereto such that each bond pad of each of the at least one pair of bond pads has only one bond wire end connected thereto, a first bond pad of the at least one pair of bond pads located in an internal portion of the semiconductor die.

2. The integrated circuit of Claim 1 wherein the at least one pair of bond pads includes a second bond pad located along a periphery of the semiconductor die.

3. The integrated circuit of Claim 1 wherein the single corresponding bond wire comprises a metallic material selected from the group consisting of gold, aluminum, and copper.

4. The integrated circuit of Claim 1 wherein the single corresponding bond wire is bonded to the pair of bond pads using a wire bond type selected from the group consisting of ball bonds, stitch bonds, stitch bonds on bonding pad, and stitch bonds on ball.

5. The integrated circuit of Claim 1 further comprising a trace in the semiconductor die connected between the pair of bond pads.

6. The integrated circuit of Claim 1 wherein the at least one pair of bond pads includes a second bond pad located in the internal portion of the semiconductor die.

7. The integrated circuit of Claim 1 wherein the single corresponding bond wire is selected from the group consisting of power interconnects, ground interconnects, and signal interconnects.

8. The integrated circuit of Claim 1 further comprising a plurality of pairs of bond pads, each of the pairs of bond pads having a corresponding wire connected therebetween such that each bond pad of the pairs of bond pads includes a single wire bond.

9. An integrated circuit, comprising:

a semiconductor die including at least one pair of electrical termination means, each pair of electrical termination means having a single corresponding means for

conducting connected thereto such that each electrical termination means of the pair of electrical termination means has only one end of any means for conducting connected thereto, a first electrical termination means of each of the at least one pair of electrical termination means located in an internal portion of the semiconductor die.

10. The integrated circuit of Claim 9 wherein the at least one pair of electrical termination means includes a second electrical termination means located along a periphery of the semiconductor die.

11. The integrated circuit of Claim 9 wherein the single corresponding means for conducting comprises a metallic material selected from the group consisting of gold, aluminum, and copper.

12. The integrated circuit of Claim 9 wherein the single corresponding means for conducting is bonded to the pair of electrical termination means using a wire bond type selected from the group consisting of ball bonds, stitch bonds, stitch bonds on bonding pad, and stitch bonds on ball.

13. The integrated circuit of Claim 9 further comprising a trace in the semiconductor die connected between the pair of electrical termination means.

14. The integrated circuit of Claim 9 wherein the at least one pair of electrical termination means includes a second electrical termination means located in the internal portion of the semiconductor die.

15. The integrated circuit of Claim 9 wherein the single corresponding means for conducting is selected from the group consisting of power interconnects, ground interconnects, and signal interconnects.

16. The integrated circuit of Claim 9 further comprising a plurality of pairs of electrical termination means, each of the pairs of electrical termination means having a corresponding means for conducting connected therebetween such that each electrical termination means of the pairs of electrical termination means includes a single wire bond.

17. A method of distributing power in a semiconductor device, comprising;

attaching at least one pair of bond pads to the semiconductor device;

connecting a single corresponding bond wire between each of the at least one pair of bond pads such that each bond pad of each of the at least one pair of bond pads has only one bond wire end connected thereto; and

locating a first bond pad of the at least one pair of bond pads in an internal portion of the semiconductor die.

18. The method of Claim 17 further comprising locating a second bond pad the at least one pair of bond pads along a periphery of the semiconductor die.

19. The method of Claim 17 wherein the single corresponding bond wire comprises a metallic material selected from the group consisting of gold, aluminum, and copper.

20. The method of Claim 17 further comprising bonding the single corresponding bond wire to the pair of bond pads using a wire bond type selected from the group consisting of ball bonds, stitch bonds, stitch bonds on bonding pad, and stitch bonds on ball.

21. The method of Claim 17 further comprising connecting a trace in the semiconductor die between bond pads of the pair of bond pads.

22. The method of Claim 17 further comprising locating a second bond pad of the at least one pair of bond pads in the internal portion of the semiconductor die.

23. The method of Claim 17 wherein the single corresponding bond wire is selected from the group consisting of power interconnects, ground interconnects, and signal interconnects.

24. The method of Claim 17 further comprising:

attaching a plurality of pairs of bond pads to the semiconductor die; and

connecting a corresponding wire between each of the pairs of bond pads such that each bond pad of the pairs of bond pads includes a single wire bond.